

This Information Note provides details to the DVB-ASI mode of operation for the GS9090B/GS9091B and is important for migration from the GS9090, GS9090A and the GS9091A. The SMPTE SDI mode does not require the application circuit recommended below.

It is possible for the internal PLL of the GS9090B/GS9091B to falsely lock to a DVB-ASI signal harmonic rather than the 270MHz fundamental. When in this state, DVB-ASI data that is output from the GS9090B/GS9091B will be invalid and the LOCKED output will be de-asserted. The LOCKED output of the GS9090B/GS9091B is only asserted when the PLL is locked AND valid DVB-ASI sync words are detected. It will remain in this de-asserted state as long as the input signal remains. Consequently, an applications circuit is used to detect this state and restart the on-chip PLL. The applications circuit detects LOCKED de-asserted for longer than ~700µs and resets the PLL by discharging the loop filter capacitor through a CMOS switch. This may be accomplished as seen in the circuit below by using a STG719 switch as a reference. Other low leakage CMOS switches may also be substituted within the circuit.

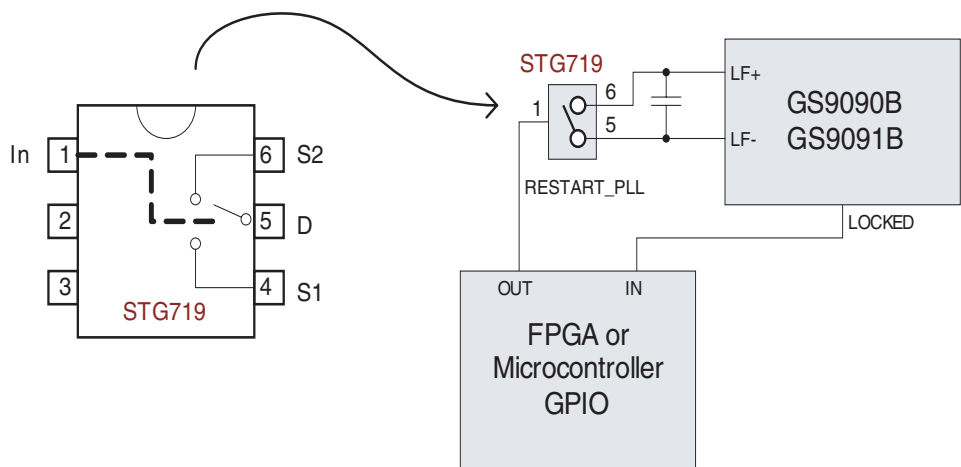


Figure 1: GS9090B/GS9091B False Lock Restart Circuit

The circuit above can be implemented using either a small state machine in an FPGA or general purpose I/O on a microcontroller in combination with some firmware. Typically, a system using the GS9090B/GS9091B will have an existing FPGA and/or microcontroller that may have some spare I/O that can be used to implement the false lock restart circuit. The choice of method will depend on what spare system resources are available. In either case, the waveform shown in Figure 2 represents how the PLL restart must be driven. The delay values of 700µs and 20µs are nominal but the values can be longer. In the case where the DDI inputs are not driven with a valid DVB-ASI signal, the RESTART_PLL signal should be repeated indefinitely as long as LOCKED remains de-asserted.

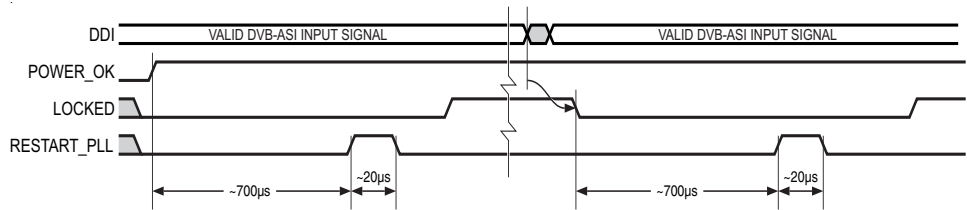



Figure 2: GS9090B/GS9091B False Lock Restart Circuit Waveforms of False Lock After Power-up and False Lock After a Signal Switch.

Revision History

Version	ECR	PCN	Date	Changes
0	140829	-	June 2006	New document created.

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