



PCI Express® to Local Bus Bridge Family GN4121 (1-lane) ~ GN4124 (4-lane)

APPLICATIONS

- High-speed data acquisition
- Video capture/DVR
- Configurable computing
- Networking and communications

GENERAL DESCRIPTION

The GN412x family of controllers are PCI Express to local bus endpoint bridges that are designed to work as companions for FPGA devices to provide a complete bridging solution for general applications. In addition to a PCI Express compliant PHY interface, the GN412x devices also contain the link and transaction layers, and an applications interface that is ideally suited to FPGA interfacing using a small number of pins. Since the PCI Express transaction/link IP is hard-wired into the GN412x, there is no need to license PCIe IP. The level of integration and very low power operation of the GN412x devices make them an ideal alternative to using a PIPE PHY, where IP licensing and the cost of FPGA resources and power consumption is unattractive by comparison. Using the GN412x allows FPGA resources to be spent on what differentiates the product rather than on implementing the PCI Express protocol.

LIVE ON POWER-UP

Since the GN412x devices contain a complete type 0 PCI configuration space, they are live on power-up so that a plug-and-play BIOS can auto-detect them and enumerate them without an attached FPGA having to be configured.

FPGA ON-THE-FLY CONFIGURATION LOADER

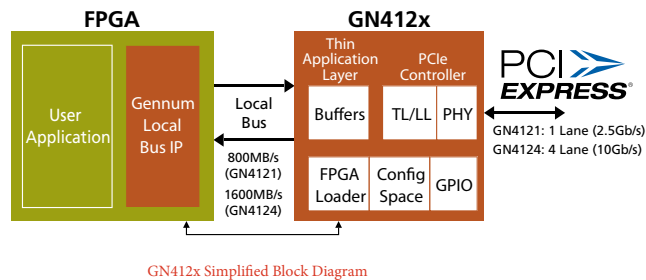
An FPGA configuration bitstream may be downloaded from the host system over PCIe to the attached FPGA using the on-chip FPGA Configuration Loader (FCL). This eliminates the expense of a dedicated FPGA ROM and makes on-the-fly reconfiguration and firmware upgrades simple. Any application requiring dynamic reconfiguration, such as configurable computing, or firmware upgrades over PCIe can benefit from the use of the GN412x as a companion device irrespective of the size or type of FPGA device used.

LOCAL BUS INTERFACE

The local bus interface uses dual data rate SSTL I/O to accomplish up to 500MB/s (GN4121) and 800MB/s (GN4124) of local bus peak throughput in each direction using the fewest possible pins (800MB/s and 1600MB/s total peak throughput). The simple local bus protocol facilitates both master mode and target mode read/write transactions. Local bus FPGA IP is licensed, and royalty free for use with the GN412x.

SCALABLE SOLUTION

The family of endpoint bridge controllers includes the GN4121 single lane (x1) device and the higher performance GN4124 4-lane (x4) device. Since the GN4121 is a software compatible, pin and functional subset of the GN4124, it is straight forward to migrate between them as desired for the price/performance requirements.



EXTEND THE REACH OF PCI EXPRESS®

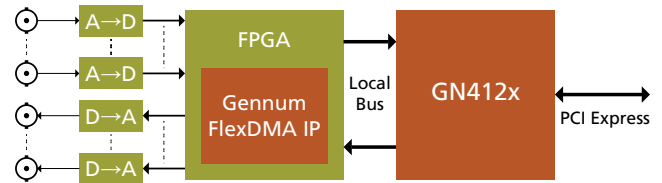
- PCI Express® interface
 - Complies with PCIe Base Specification 1.1
 - PCI SIG compliance tested
 - On-chip PHY, transaction, and link layer eliminates the cost of IP licensing
- Local bus interface
 - Supports full-duplex local bus data transfer
 - Uses SSTL dual data rate I/O for high-speed data transfer using minimum pins
 - FPGA source code provided for master/target read/write buses for easy user logic attachment
 - Local bus may be operated asynchronously to the PCIe clock rate for power optimization
- “Live” on power up
 - On-chip type 0 PCI configuration space enables auto detection without FPGA activity
 - On-chip extended configuration space supports power management, serial, number MSI, and PCIe capability registers
- FPGA bitstream loader
 - Allows easy configuration of the attached FPGA through PCIe
 - Provides on-the-fly FPGA reconfiguration capability
- I²C master/target
- INTx and MSI Interrupt controller
- 2kV ESD protection
- 256 pin 17mm x 17mm lead-free BGA
- 0-85°C operating temperature

EXAMPLE APPLICATIONS

Due to the general purpose nature and flexibility of the GN412x, many applications can be supported.

DATA ACQUISITION

Data acquisition over PCI Express is easily implemented with the GN412x and the FlexDMA FPGA IP core. The FlexDMA IP core from Gennum supports up to 256 channels of scatter/gather DMA in each direction (512 total). Since the GN412x provides full duplex traffic via the local bus, simultaneous inputs and outputs can take advantage of the full duplex nature of PCI Express.



Data Acquisition Using the GN412x

GN4121/GN4124 FEATURE/COMPARISON CHART

	GN4124	GN4121
PCI Express Lanes	x4 at 2.5Gb/s (10Gb/s)	x1 at 2.5Gb/s
# of Virtual Channels	2	1
Peak Local Bus Throughput	1600MB/s (800MB/s in each direction)	1000MB/s (500MB/s in each direction)
Peak System Throughput	1600MB/s (800MB/s in each direction)	500MB/s (250MB/s in each direction)
Local Bus IO Count	54	49
GPIO	16 (optional)	
PCI SIG Compliance Tested	Yes, on PCI SIG Integrators List	
Max Payload Size	512	
“Live” On Power-up	Yes	
I ² C Master/Target	Enables application specific information such as BAR sizes, Subsystem ID, and Subsystem Vendor ID to be customized using a small EEPROM. Allows an external I ² C master to access internal registers.	
Power Dissipation (typ/max)	650mW / 950mW	475mW / 695mW
FPGA Bitstream Loader	Yes, FPGA loader utility with source code provided	
Local Bus Clock Speed (max)	200MHz (DDR)	125MHz (DDR)
On-chip Configuration Space	Yes, Type 0 config space, config and extended registers are available through BAR4	
Package	256 pin 17mm x 17mm lead-free BGA, Green	
Local Bus IP	Royalty free source code provided. Supports master/target interfaces with FlexDMA scatter/gather DMA controller for up to 256 channels in each direction. Supports simultaneous DMA in both upstream and downstream direction.	
Interrupt Controller	Supports INTx and MSI, can convert hardwired interrupt into PCIe INTx/MSI	
Software/Driver	“GenDiag” diagnostic/benchmark software provided with source code, uses either a native Linux driver or uses Jungo WinDriver DDK that supports Windows 2000/XP/XP Embedded /Server 2003, Vista, Windows CE / Mobile, Linux, Solaris and VxWorks. A WDM driver using DirectShow for Video capture is also available.	
Software/IP Updates	Documentation, evaluation board/schematics, FPGA IP, example FPGA application code, driver software, application notes available to qualified registered users at www.gennum.com/mygennum	

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