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PROCESS/PRODUCT CHANGE NOTICE

Issuing Division:	Analog and Mixed Signal Products
Part Family Affected:	Gennum's PCI Express products
Part Numbers Affected:	GN4124 A1 Stepping
Date Code / Lot No.:	N/A
Type of Change:	<input type="checkbox"/> Type 1: Process <input checked="" type="checkbox"/> Type 2: Product Features and/or Specifications <input type="checkbox"/> Type 3: Product Obsolete with/without replacement <input type="checkbox"/> Type 4: Recommended Applications Circuit Changes <input type="checkbox"/> Type 5: Datasheet Only <input type="checkbox"/> Type 6: Shipping/Packing Method
Title of Change:	GN4124 Errata
Date of Issue:	November 20, 2008
Effective Date:	November 20, 2008
Authorized by:	Mike Alford, Market Manager, Computing
PCN Number:	51624
Datasheet Revision:	N/A

First Target Mode TWI (I2C) Access Overwrites Vendor/Device ID Register

DESCRIPTION OF CHANGE:

The TWI controller has a target mode of operation that allows an external TWI master to access registers inside the GN4124. Target mode is enabled after device reset and after EEPROM initialization. Once target mode is enabled, the first access (read or write) to the GN4124 via external master (such as the FPGA or a processor) causes the address of the read or write to be written into the register at offset 0x00 as data. These are the Vendor/Device ID registers. Only the first target access is problematic and all subsequent access function as expected.

EFFECT OF CHANGE:

Low Impact. Most applications don't use TWI target mode except for debugging purposes. Mostly the TWI is used in boot master mode to pre-configure register values such as subsystem/subsystem vendor ID for proper Plug-and-Play driver detection. This mode is fully functional.

RECOMMENDED CUSTOMER ACTION(S):

A workaround is only required if TWI target mode is being used. In this case, it is recommended to re-write the Vendor/Device ID. However, if TWI target mode is used only after OS boot then vendor/device ID is already known to the OS and it may not be necessary to re-write the values. The value of the Vendor/Device ID register doesn't affect the internal operation of the GN4124 and is only used by the OS for Plug-and-Play detection.

This erratum will not be fixed in the next revision of the silicon.

Local Bus FIFO Thrashing Causes Performance Degradation

DESCRIPTION OF CHANGE:

The local bus interface has FIFOs (Tx and Rx) that transmit/receive local bus packets. This erratum involves the behaviour of those FIFOs.

Local-to-PCIe direction: When an attached FPGA sends sufficiently long packets via the L2P interface, the L2P_RDY signal will be de-asserted for short periods of time. This causes data flow from the FPGA to be throttled and the FPGA must de-assert L2P_VALID and effectively stall the data transfer until L2P_RDY is re-asserted. The net result is that for long packets, the utilization of the bus is reduced by about 65%. However, data transfer remains intact and robust.

PCIe-to-Local direction: The GN4124 may de-assert P2L_VALID for brief periods of time even if the P2L_RDY remains asserted. The net result is similar to the Local-to-PCIe direction: the utilization of the bus is reduced by about 65%. Only performance is affected and no loss of data occurs.

EFFECT OF CHANGE:

High impact for applications that need 4-lane level of performance. 1-lane applications will not suffer performance degradation.

RECOMMENDED CUSTOMER ACTION(S):

The Gennum local bus IP has been designed to minimize the impact of the errata. However, there is no way to completely overcome the performance degradation.

For single lane PCI Express applications, there is no performance degradation when the local bus is operated at 100MHz and above.

This erratum will be fixed in the A2 stepping of the silicon so that continuous data bursting is sustained. No changes to customer IP will be required and designs developed for the GN4124 A1 stepping will operate un-modified but with increased throughput.

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